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BUFFERED OVERSAMPLING ANALOG-TO-DIGITAL CONVERTER WITH IMPROVED DC OFFSET PERFORMANCE

Background of the Invention

[0001] Converting a continuous-time analog signal to a discrete-time digital representation typically requires anti-alias filtering, sampling and quantization. An anti-aliasing filter ensures that analog input signal is properly band-limited prior to sampling. A sampler captures samples of the filtered input signal at discrete time intervals $T = 1/F_s$, where F_s is the sampling frequency. Sampling frequency F_s typically is selected as at least twice the bandwidth of the filtered analog input signal. A quantizer converts the samples to a discrete set of values. Conventional analog-to-digital (A/D) converters typically perform sampling and quantization, whereas separate discrete components or integrated circuits perform anti-aliasing.

[0002] Oversampling A/D converters, in contrast, sample an analog input signal at a rate NF_s that is many times greater than twice the bandwidth of the analog input signal. An oversampling converter typically includes an anti-alias filter, a sampler and modulator

(quantizer), and a digital filter. The sampler and quantizer operate at the elevated rate NF_s. The digital filter, typically called a decimator, provides low-pass filtering to suppress signals above $F_s/2$, and sample-rate reduction to lower the sample rate to the desired rate F_s. As a result of the higher input sampling rate, over-sampling converters have less stringent anti-alias filter requirements than traditional converters. In addition, oversampling converters permit lower quantization noise power, and hence improved signal-to-noise ratio compared to traditional converters.

[0003] One key requirement for oversampling A/D converters is low DC offset. If the input to an oversampling A/D converter is zero (e.g., 0 volts), the output of the converter ideally is a digital code corresponding to zero. As a result of component mismatches, however, the output of a real A/D converter to a zero input is a digital code that corresponds to a value other than zero. The magnitude of the converter's input-referred DC offset is the magnitude of the DC input signal that causes the A/D converter to produce a zero output. The DC offset of the converter may vary with time and temperature. This phenomenon typically is called "offset drift." Another key requirement for oversampling A/D converters is low offset drift with time and temperature.

[0004] Previously known techniques have been used to improve the DC offset performance of A/D converters. For example, Donald A. Kerth et al., "An Oversampling Converter for Strain Gauge Transducers," IEEE J. Solid State Circuits, 27(12):1689-96 (Dec. 1992), describes an oversampling Δ-Σ A/D converter architecture that uses chopper-stabilized amplifiers to substantially

reduce the overall DC offset of the converter. Nevertheless, the non-ideal chopper amplifier switches contribute DC offset and offset drift proportional to the chopper frequency, which corresponds to the relatively high sampling frequency of the Δ-Σ modulator. Although digital calibration techniques may be used to remove residual DC offset, such techniques are ineffective for correcting offset drift. Further, to increase the converter's resolution, the sampling frequency of the Δ-Σ modulator may be increased. Such increases, however, require that the chopper frequency also must increase, which increases residual offset and offset drift.

[0005] An improved offset performance A/D converter is described in Damien McCartney et al., "A Low-Noise Low Drift Transducer ADC," IEEE J. Solid State Circuits, 32(7):959-967 (Jul. 1997) ("McCartney"). The architecture of the McCartney converter is shown in FIG. 1. Converter 10 includes analog chopper 12, buffer amplifier 14, Δ-Σ modulator 16, digital chopper 18, $Sinc^3$ filter and decimator 20, and FIR filter 22. Analog chopper 12 chops analog input signal V_{IN} with a square wave of frequency f_{chop}. For example, as described by McCartney, if V_{IN} is a differential signal, analog chopper 12 may be implemented as a multiplexer that successively reverses the polarity of V_{IN}. Buffer amplifier 14 isolates the chopped analog input signal from the succeeding switched capacitor circuitry, and may provide adjustable gain. Δ-Σ modulator 16 samples the output of buffer amplifier 14 at a frequency f_{mod} that is much higher than chop frequency f_{chop}, and provides a digital data stream at

its output. For example, $f_{mod} = 2 \times N \times f_{chop}$, where N is the oversampling ratio of Δ-Σ modulator 16. Digital chopper 18 is phase-synchronized with analog chopper 12, and chops the digital data output of Δ-Σ modulator 16 to provide a digital data steam at a rate f_{mod}. Sinc^3 filter and decimator 20 filter and decimate the output data stream of digital chopper 18 to provide a digital stream x(n) at a rate f_{mod}/N.

[0006] If chopper frequency f_{chop} equals $f_{mod}/(2 \times N)$, then successive samples $x(n)$ provided at the output of Sinc^3 filter and decimator 20 are digital representations of the analog signals $(V_{IN} + V_{OS})$ and $(V_{IN} - V_{OS})$, where V_{OS} is the input-referred offset of buffer amplifier 14 and Δ-Σ modulator 16. For example, x(n) for n = 0, -1, -2, -3, -4, may be expressed as:

$$\begin{aligned}
x(0) &= (V_{IN}(0) + V_{OS}(0)) \\
x(-1) &= (V_{IN}(-1) + V_{OS}(-1)) \\
x(-2) &= (V_{IN}(-2) + V_{OS}(-2)) \\
x(-3) &= (V_{IN}(-3) + V_{OS}(-3)) \\
x(-4) &= (V_{IN}(-4) + V_{OS}(-4))
\end{aligned} \tag{1}$$

where $V_{IN}(n)$, n = 0, -1, -2, -3, -4, . . ., are samples of input signal V_{IN}, and $V_{OS}(n)$, n = 0, -1, -2, -3, -4, . . ., are samples of input-referred offset V_{OS}.

[0007] FIR filter 22 removes V_{OS} from output x(n) of Sinc^3 filter and decimator 20 and provides digital output signal y(n) at rate f_{chop}. If FIR filter 22 has L coefficients h(n), n = 0, 1, 2, . . ., L-1, output y(n) may be expressed as:

$$y(n)=\sum_{k=0}^{L-1} h(k)\times(n-k) \tag{2}$$

For example, if L = 2, output y(n) may be expressed as:

$$y(n) = h(0)x(n) + h(1)x(n-1) \tag{3}$$

For n = 0, y(0) equals:

$$y(0) = h(0)x(0) + h(1)x(-1) \tag{4a}$$

$$= h(0)[V_{IN}(0) + V_{OS}(0)] + h(1)[V_{IN}(-1) - V_{OS}(-1)) \tag{4b}$$

If f_{chop} is many times higher than twice the bandwidth of V_{IN} and V_{OS}, then

$$V_{IN}(0) \approx V_{IN}(-1) \tag{5a}$$

$$V_{OS}(0) \approx V_{OS}(-1) \tag{5b}$$

Ideally, y(n) contains no offset V_{OS}, such that

$$y(n) = V_{IN}(n) \tag{6}$$

Combining equations (4b), (5) and (6), impulse response coefficients h(0) = +0.5 and h(1) = +0.5.

[0008] An alternative embodiment of the converter of FIG. 1 is shown in FIG. 2. Circuit 30 includes excitation source 32, analog chopper 34, sensor 36 and A/D converter 38. Excitation source provides analog excitation input signal E_{IN}, and sensor 36 may be, for example, a resistor bridge strain gauge used in an industrial weigh scale. Analog excitation input signal E_{IN} typically is a DC signal. Analog chopper 34 chops

analog excitation input signal E_{IN}, and provides the chopped signal to resistor bridge 36. The analog output of resistor bridge 36 is the input to A/D converter 38. A/D converter 38 includes chop synch 40, which provides analog chopper 34 with a clock signal of the correct polarity and phase to synchronize analog chopper 34 to A/D converter 38. By including sensor 36 in the chop loop, circuit 30 removes offsets in sensor 36 caused by thermal electromotive force (EMF) or leakage current. As described by McCartney, Δ-Σ modulator 16 may be implemented as a 1-bit Δ-Σ modulator, and digital chopper 18 may be implemented as an exclusive-OR gate.

[0009] To provide lower quantization error, it may be desirable to implement Δ-Σ modulator 16 as a multi-bit Δ-Σ modulator (i.e., a modulator that provides a multi-bit digital output data stream). Alternatively, it may be desirable to implement modulator 16 using other oversampling quantizer architectures (e.g., successive approximation, flash, or pipelined quantizers) that provide multi-bit digital representations of the signal applied to the quantizer's input. In such multi-bit implementations, digital chopper 18 may not be implemented using a simple exclusive-or gate, but instead requires more complex circuitry.

[0010] In various real-world applications, sensors of physical quantities are connected to ADCs. However, due to fluctuations in the input impedance of the ADCs as a result of the signal sampling process, the ADCs must be preceded by relatively high impedance signal processing chains to maintain the accuracy of the ADCs.

For high accuracy oversampling converters (i.e., converters that evaluate the input signal at rates much higher than the conversion rate) this presents a difficult requirement.

[0011] A variety of solutions have been proposed to achieve relatively high and relatively constant impedance of high accuracy oversampling ADCs. Several of these solutions have included integrated input buffers. However, in each of these proposed solutions that include an input buffer, a compromise is met between DC accuracy and input noise level. For example, low noise level is chosen at the expense of DC accuracy or vice-versa.

[0012] It therefore would be desirable to provide an oversampling analog-to-digital converter that has reduced DC offset and offset drift and relatively high and constant input impedance.

[0013] It further would be desirable to provide an oversampling analog-to-digital converter that has reduced DC offset and offset drift and relatively high and constant input impedance, but that does not require a digital chopper stage.

[0014] It is therefore also desirable to provide an analog-to-digital converter that provides for the use of a low noise external amplifier/buffer while still maintaining exceptional DC accuracy for the overall converter.

Summary of the Invention

[0015] Accordingly, it is an object of this invention to provide an oversampling analog-to-digital converter that has reduced DC offset and offset drift and relatively high and constant input impedance.

[0016] It further is an object of this invention to provide an oversampling analog-to-digital converter that has reduced DC offset and offset drift and relatively high and constant input impedance, but that does not require a digital chopper stage.

[0017] It further is an object of this invention to provide an analog-to-digital converter that provides for the use of a low noise external amplifier/buffer while still maintaining exceptional DC accuracy for the overall converter.

[0018] In accordance with the principles of this invention, a user can optimize an A/D converter for the specific application required. The user can optimize the converter by inserting a customized buffer/amplifier between an analog chopper and a signal processing chain. The customized buffer/amplifier is optimized for input noise and the signal chain compensates for poor DC performance. The result is a buffered analog-to-digital converter with both low input noise and very good DC accuracy.

Brief Description of the Drawings

[0019] The above-mentioned objects and features of the present invention can be more clearly understood from the following detailed description considered in conjunction with the following drawings, in which the same reference numerals denote the same structural elements throughout, and in which:

[0020] FIG. 1 is a block diagram of a previously known A/D converter circuit;

[0021] FIG. 2 is a block diagram of another previously known A/D converter circuit;

[0022] FIG. 3 is a block diagram of another previously known A/D converter circuit;

[0023] FIG. 4 is a schematic diagram of exemplary analog chopper circuitry of FIG. 3;

[0024] FIG. 5 is a block diagram of another previously known A/D converter circuit;

[0025] FIG. 6 is a block diagram of an A/D converter circuit of this invention;

[0026] FIG. 7 is a block diagram of another A/D converter circuit of this invention; and

[0027] FIG. 8 is a diagram of frequency response.

Detailed Description of the Invention

[0028] Referring to FIG. 3, an A/D converter is described. A/D converter 50 includes analog chopper 12', buffer amplifier 14, quantizer 52, digital filter and $decimator_1$ 54, FIR filter 56 and $decimator_2$ 58.

[0029] Analog chopper 12' chops analog input signal V_{IN} with a square wave of frequency f_{chop}, which successively reverses the polarity of V_{IN}. Analog chopper 12' may be implemented using any well-known analog chopping circuitry. For example, as shown in FIG. 4, if input signal V_{IN} is a differential signal $V_{IN} = (V_{IN}^+ - V_{IN}^-)$, analog chopper 12' may be implemented using cross-coupled switches 24, 25, 26, and 27. Switch 26 is controlled by complementary chop signal $\bar{Q}$, and is coupled between V_{IN}^+ and V_{COUT}^-. Switch 27 is controlled by complementary chop signal $\bar{Q}$, and is coupled between V_{IN}^- and V_{COUT}^+. Chop signals Q and $\bar{Q}$ are complementary logic signals of frequency f_{chop}. For example, when Q is HIGH and $\bar{Q}$ is LOW, $V_{COUT}^+ = V_{IN}^+$, and $V_{COUT}^- = V_{IN}^-$. When $\bar{Q}$ is HIGH and Q is LOW, $V_{COUT}^+ = V_{IN}^-$ and

$V_{COUT}^- = V_{IN}^+$. Analog chopper 12' alternatively may be implemented using multiplexer circuitry as described by McCartney, analog multiplier circuitry, or any other suitable analog chopper circuitry.

[0030] Buffer amplifier 14 couples the output of analog chopper 12' to quantizer 52, which may be any conventional oversampling quantizer, such as a single or multi-bit Δ-Σ modulator, successive approximation quantizer, flash quantizer, pipelined quantizer, or other suitable oversampling quantizer. Quantizer 52 provides a digital output at a rate f_{quant} that is substantially higher than f_{chop}.

[0031] The digital output of quantizer 52 is the input to digital filter and decimator$_1$ 54, which includes a digital filter and a decimator that reduces the output data rate by a factor of M. For example, digital filter and decimator$_1$ 54 may be implemented using Sinc^3 filter and decimator 20 (FIG. 1), in which M equals the oversampling ratio N of quantizer 52. Alternatively, digital filter and decimator$_1$ 54 may be any other suitable digital filter and decimator.

[0032] Digital filter and decimator$_1$ 54 provide an output sequence x'(n) at a rate f_{quant}/M. If control frequency f_{chop} to analog chopper 12' equals $f_{quant}/(2\times M)$, then successive output samples x'(n) of digital filter and decimator$_1$ 54 are digital representations of the analog signals $(V_{IN} + V_{OS})$ and $-(V_{IN} - V_{OS})$, where V_{OS} is the input-referred offset of buffer amplifier 14 and quantizer 52. For example, x'(n) for n = 0, -1, -2, -3, -4 may be expressed as:

$$x'(0) = +(V_{IN}(0) + V_{OS}(0))$$
$$x'(-1) = -(V_{IN}(-1) - V_{OS}(-1))$$

$x'(-2) = +(V_{IN}(-2) + V_{OS}(-2))$
$x'(-3) = -(V_{IN}(-3) - V_{OS}(-3))$
$$x'(-4) = +(V_{IN}(-4) + V_{OS}(-4)) \quad (7)$$

Comparing equations (1) and (7), sequence x'(n) may be expressed as:

$$x'(n) = (-1)^n x(n), \quad n = 0, -1, -2, \ldots \quad (8)$$

FIR filter 56 removes V_{OS} from sequence x(n). If FIR filter 56 has L coefficients h'(n), n = 0, 1, 2, . . ., L-1, output z'(n) of FIR filter 56 may be expressed as:

$$z'(n) = \sum_{k=0}^{L-1} h'(k) \times' (n-k) \quad (9)$$

Combining equations (8) and (9), output z'(n) may be expressed as:

$$z'(n) = (-1)^n \sum_{k=0}^{L-1} (-1)^{-k} h'(k) \times (n-k) \quad (10)$$

[0033] Decimator$_2$ 58 reduces the data rate by a factor P, which is an even integer greater than or equal to 2. That is, from every block of P successive samples z'(n), decimator$_2$ 58 provides the first sample at its output y'(n), and discards the remaining P-1 samples. Output y'(n) is at a rate $f_{quant}/(M \times P)$. For example, if P = 2, output y'(n) is at a rate f_{chop}.

[0034] Because P is an even integer, the phase relation between analog chopper 12' and decimator$_2$ 58 may be set so that y'(n) is chosen for n always even or

n always odd. If n is even, output y'(n) may be expressed as:

$$y'(n) = \sum_{k=0}^{L-1} (-1)^{-k} h'(k) \times (n-k) \tag{11}$$

Ideally, y'(n) contains no offset V_{OS}, such that

$$y'(n) = V_{IN}(n) \tag{12}$$

From equations (2), (6), (11) and (12), therefore,

$$\sum_{k=0}^{L-1} h(k) \times (n-k) = \sum_{k=0}^{L-1} (-1)^{-k} h'(k) \times (n-k) \tag{13}$$

and therefore coefficients h'(n) may be expressed as:

$$h'(n) = (-1)^n h(n),\ n = 0, 1, 2, \ldots, L-1 \tag{14}$$

Thus, for n even, coefficients h'(n) of FIR filter 56 equal coefficients h(n) of prior art FIR filter 22, but with the sign reversed for all odd coefficients.

[0035] Alternatively, if n is odd, output y'(n) may be expressed as:

$$y'(n) = \sum_{k=0}^{L-1} (-1)^{-(k-1)} h'(k) \times (n-k) \tag{15}$$

Ideally, y'(n) contains no offset V_{OS}, such that

$$y'(n) = V_{IN}(n) \tag{16}$$

From equations (2), (6), (15) and (16), therefore,

$$\sum_{k=0}^{L-1} h(k) \times (n-k) = \sum_{k=0}^{L-1} (-1)^{-(k-1)} h'(k) \times (n-k) \tag{17}$$

and therefore coefficients h'(n) may be expressed as:

$$h'(n) = (-1)^{n-1} h(n),\ n = 0,\ 1,\ 2,\ \ldots,\ L\text{-}1 \tag{18}$$

Thus, for n odd, coefficients h'(n) of FIR filter 56 equal coefficients h(n) of prior art FIR filter 22, but with the sign reversed for all even coefficients.

[0036] FIG. 5 illustrates another converter circuit of this invention that includes a sensor within the chopped conversion chain. Circuit 60 includes excitation source 32, analog chopper 34' and sensor 36, and A/D converter 62. A/D converter 62 includes chop synch 40 (as in FIG. 2), and includes buffer amplifier 14, quantizer 52, digital filter and $decimator_1$ 54, FIR filter 56 and $decimator_2$ 58 (as in FIG. 3). Converter 60 reduces thermal EMF errors due to sensor interconnects and also reduces offset, offset drift and 1/f noise errors produced by buffer amplifier 14 and quantizer 52.

[0037] Referring to FIG. 6, an improved A/D converter in accordance with the principles of the present invention is described. Like reference numerals in FIGS. 3 and 5 refer to like components in FIGS. 6 and 7.

[0038] A/D converter 50 of FIG. 6 includes analog chopper 12', quantizer 52, digital filter and

decimator$_1$ 54, FIR filter 56, and decimator$_2$ 58. In addition, A/D converter 50 includes chopper output 13 and quantizer input 15. Buffer amplifier 14 is not present in A/D converter 50 of FIG. 6.

[0039] By inserting a customized buffer/amplifier between chopper 12' and quantizer 52, a user can optimize A/D converter 50 for the specific application required. The input of the customized buffer/amplifier can be coupled to the output of chopper 12' at first terminal 13, and the output of the customized buffer/amplifier can be coupled to the input of quantizer 52 at second terminal 15. The customized buffer/amplifier should be optimized for input noise, bandwidth, and signal amplitude.

[0040] The operation of the signal processing chain (chopper 12', quantizer 52, digital filter and decimator$_1$ 54, FIR filter 56, and decimator$_2$ 58) will compensate for buffer/amplifier poor DC performance. The result of inserting a customized buffer/amplifier is a buffered analog-to-digital converter with both very low input noise and very good DC accuracy.

[0041] Referring to FIG. 6, another improved A/D converter in accordance with the principles of the present invention is described. Circuit 60 includes a sensor within a chopped conversion chain. Circuit 60 includes excitation source 32, analog chopper 34', sensor 36, and A/D converter 62.

[0042] As in FIG. 5, A/D converter 62 of FIG. 7 includes chop synch 40, quantizer 52, digital filter and decimator$_1$ 54, FIR filter 56, and decimator$_2$ 58. However, converter 62 of FIG. 7 does not include buffer amplifier 14.

[0043] By inserting a customized buffer/amplifier between sensor 36 and quantizer 52 of FIG. 7, a user can optimize the A/D converter for the specific application required. The input of the customized buffer/amplifier can be coupled to the output of sensor 36 at first terminal 38 and the output of the customized buffer/amplifier can be coupled to the input of quantizer 52 at second terminal 48. The customized buffer/amplifier should be optimized for input noise, bandwidth, and signal amplitude. The operation of the signal processing chain (chopper 34', quantizer 52, digital filter and decimator$_1$ 54, FIR filter 56, and decimator$_2$ 58) will compensate for buffer/amplifier poor DC performance. The result of inserting a customized buffer/amplifier is a buffered analog-to-digital converter with both very low input noise and very good DC accuracy.

[0044] In another aspect of the invention, a method of attenuating a converted digital signal over a wide null band -- e.g., from 48Hz to 62Hz -- is provided. Using conventional methods to produce a wide null band requires complex filter circuitry that is difficult to fabricate and occupies a substantial amount of die space. In a method for producing a wide null band according to the invention, the band is produced using substantially fewer components and less complex circuitry than by conventional methods.

[0045] Two examples of circuits which can be used to implement the method according to the invention are shown in FIGS. 1 and 3. To produce the desired null band, this method requires only a cascade connection of the two digital filters/decimators. Therefore, the method of the invention can operate with or without the

second digital chopper 18 (as in the circuit shown in FIG. 1) or by modifying the sign of the coefficients of the second digital filter/decimator (as in the circuit in FIG. 3).

[0046] More specifically, the circuit shown in FIG. 1 can be used in a method according to the invention by implementing FIR filter 22 with two equal coefficients of 1/2{h(0)=h(1)=.5} and, filter 20 as a $sinc^4$ filter. Alternatively, the method can be implemented using the circuit shown in FIG. 3. To accomplish this, the digital filter/decimator 54 can be implemented as a $sinc^4$ with an impulse response of total length 4*k and a decimation factor M=4*k ($F_1=F_s/(4*k)$) and the digital filter/decimator 58 can be implemented as an FIR of length 2 with coefficients h(0)=-h(1)=0.5 or h(0)=-h(1)=-0.5 and decimation factor P = 2 ($F_{out}=F_s/(8*k)$). The actual value of k typically has little influence over the described invention. Nevertheless, a common value selected in such configurations is k = 256. The notch, or center, frequency F_o can again be defined as $F_o = F_s/k$.

[0047] The attenuation of the input signal magnitude around the notch frequency, F_o, due to such an implementation can be written as:

$$H(f) = 20\times\log_{10}\left|\left(\frac{\sin(\pi\times f/Fo)}{k\times\sin(\pi\times f/k\times Fo)}\right)^4\times \frac{\sin(8\times\pi\times f/Fo)}{2\times\sin(4\times\pi\times f/Fo)}\right| \quad (19)$$

[0048] It should be noted that the method according to invention is not limited to these particular circuit configurations but, rather, these are only exemplary

configurations of circuits that produce the results required by the method of the invention.

[0049] FIG. 8 shows one preferable frequency response that is obtainable according to the method of the invention. In this particular response, an F_{clk} signal is selected such that F_s = 55*k Hz, which provides a corner frequency of $F_o = F_s/k$ = 55Hz. It is shown in FIG. 8, that an implementation according to the invention provides better than about 87 dB of input perturbation rejection in a frequency range of 48Hz (=50Hz-4%) to 62.5Hz (=60Hz+4%), or about +-14% of the corner frequency. For many applications, this level of rejection is sufficient. Furthermore, in this particular embodiment, attenuation that extends about +-14% around a center frequency of about 55Hz, or other center frequency chosen to provide coverage of the 50Hz and 60Hz power line frequencies, also provides a substantial advantage. It should be noted that the invention is not limited to this particular range.

[0050] Persons skilled in the art further will recognize that the circuitry of the present invention may be implemented using circuit configurations other than those shown and discussed above. All such modifications are within the scope of the present invention, which is limited only by the claims that follow.